

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
21 August 2003 (21.08.2003)

PCT

(10) International Publication Number
WO 03/069413 A1

- (51) International Patent Classification⁷: **G03F 7/20, 7/00**
- (21) International Application Number: **PCT/US02/13442**
- (22) International Filing Date: **29 April 2002 (29.04.2002)**
- (25) Filing Language: **English**
- (26) Publication Language: **English**
- (30) Priority Data:
10/074,562 12 February 2002 (12.02.2002) US
- (71) Applicant (*for all designated States except US*):
IRIDIGM DISPLAY CORPORATION [US/US];
Suite 235, 2415 Third Street, San Francisco, CA 94107 (US).
- (72) Inventor; and
- (75) Inventor/Applicant (*for US only*): **MILES, Mark, W.**
[US/US]; Building 43, Fort Mason, San Francisco, CA 94123 (US).
- (74) Agents: **MALLIE, Michael, J. et al.;** Blakely, Sokoloff,
Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZM, ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

WO 03/069413 A1

(54) Title: A METHOD FOR FABRICATING A STRUCTURE FOR A MICROELECTROMECHANICAL SYSTEMS (MEMS) DEVICE

(57) Abstract: The invention provides a microfabrication process which may be used to manufacture a MEMS device. The process comprises depositing one or a stack of layers on a base layer, said one layer or an uppermost layer in said stack of layers being a sacrificial layer; patterning said one or a stack of layers to provide at least one aperture therethrough through which said base layer is exposed; depositing a photosensitive layer over said one or a stack of layers; and passing light through said at least one aperture to expose said photosensitive layer.

BEST AVAILABLE COPY

A METHOD FOR FABRICATING A STRUCTURE FOR A MICROELECTROMECHANICAL SYSTEMS (MEMS) DEVICE

FIELD OF THE INVENTION

[0001] This invention relates to microfabrication. In particular, it relates to the microfabrication of a structure for a Microelectromechanical Systems (MEMS) device.

BACKGROUND

[0002] Microfabrication techniques used to fabricate MEMS devices generally involve the deposition of one or more layers on a substrate and the subsequent patterning of the layers to produce useful structures. One technique for patterning a layer involves the use of photolithography. With photolithography a photographic definition of a desired pattern on a photo or optical mask is used to impart the pattern onto a surface of the layer. When manufacturing a MEMS device usually several masking steps are required, each masking step adding to the cost of the device. Accordingly, it is desirable to reduce the number of masking steps required during fabrication of a MEMS device.

SUMMARY OF THE INVENTION

[0003] According to one aspect of the invention there is provided a microfabrication process comprising depositing a first layer on a substrate; patterning the first layer; depositing a second layer on the first layer; and patterning the second layer using the first layer as a photomask.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figure 1 shows a three dimensional drawing of a part of a MEMS device which may be manufactured using the microfabrication process of the present invention; and

[0005] Figures 2 to 10 shows various stages in the manufacture of the MEMS device of Figure 1.

DETAILED DESCRIPTION

[0006] Aspects of the present invention will now be described with reference to Figures 2 to 10 of the drawings which show the stages during fabrication of a MEMS device such as a Visible Spectrum Modulator Array described in U.S. Patent No. 5,835,255 or an Interferometric Modulator (IMOD) described in U.S. Patent No. 6,040,937. Naturally, describing the present invention with reference to stages in the manufacture of a Visible Spectrum Modulator Array or an IMOD is intended to enhance understanding of the present invention and it is to be understood that the present invention may be used in the manufacture of other MEMS devices. Thus, the description of the present invention with reference to the manufacture of a Visible Spectrum Modulator Array or an IMOD is intended to be non-limiting.

[0007] Figure 1 of the drawings shows an example of a part of a Visible Spectrum Modulator Array 10 which may be fabricated in accordance with techniques described herein. Referring to Figure 1, an antenna array is fabricated on one-half of a microfabricated interferometric cavity which transmits and reflects certain portions of incident electromagnetic radiation depending on (a) the dimensions of the cavity itself and (b) the frequency of response of dielectric mirrors in the cavities. In Figure 1, the array 10 is shown to include two cavities 12, 14 fabricated on a transparent substrate 16. A layer 18, the primary mirror/conductor may comprise a combination of one or more films of metals, oxides, semiconductors, and transparent conductors. Insulating supports 20 hold up a second transparent conducting membrane 22. Each array element has an antenna array 24 formed on the membrane 22. The two structures 22, 24, together comprise the secondary mirror/conductor. Conversely, the antenna array may be fabricated as part of the primary mirror/conductor. Secondary, mirror/conductor 22/24 forms a flexible membrane, fabricated such that it is under tensile stress and thus parallel to the substrate, in an undriven state.

[0008] Because layers 22 and 24 are parallel, radiation which enters any of the cavities from above or below the array can undergo multiple reflections within the cavity, resulting in optical interference. Depending on the

dimensions of the antenna array, the interference will determine its reflective and/or transmissive characteristics. Changing one of the dimensions, in this case the cavity height (i.e. the spacing between the inner walls of layers 18, 22), will alter the optical characteristics. The change in height is achieved by applying a voltage across the two layers of the cavity, which due to electrostatic forces, causes layer 22 to collapse. Cavity 12 is shown collapsed (7 volts applied), while cavity 14 is shown uncollapsed (0 volts applied).

[0009] In fabricating the array 10, it is desirable that insulating supports 20 are well defined in regions where contact is made between insulating supports 20 and layers 18, 22. The present invention is especially useful in manufacturing such a support. Figures 2 through 10 show various stages in the manufacture of a MEMS device having supports such as the supports 20. Referring to Figure 2 of the drawings, reference numeral 100 indicates a substrate 100. The substrate 100 may be of many different materials each being transparent to ultraviolet light. Examples of these materials include plastic, mylar, or quartz. The material must be able to support an optically smooth, though not necessarily flat, finish. A preferred material would likely be glass, which would be both transmissive and reflective operation in the visible range.

[0010] Various layers are deposited on substrate 100 to define a stack. In particular, the substrate 100 is coated with a sacrificial layer 102 using standard techniques such as a physical vapor deposition (PVD) method such as sputtering or e-beam evaporation. Other possible methods include chemical vapor deposition and molecular beam epitaxy.

[0011] In Figure 2, the sacrificial layer is a single layer. However, in other embodiments of the invention layer 102 may be a stack of layers with an uppermost sacrificial layer.

[0012] Figure 3 of the drawings shows a stage in the manufacture of the MEMS device wherein the sacrificial layer 102 has been patterned so as to define longitudinally spaced grooves 104. A standard procedure is used to pattern sacrificial layer 102 which includes exposing layer 102 through an appropriate mask and developing to produce the pattern.

[0013] In Figure 4 of the drawings, a photosensitive polymeric material in the form of a negative-acting-photosensitive material which could be a negative photoresist has been spun onto sacrificial layer 102 with a thickness that is larger than the total height of the film stack defined by layers 100 and 102. Thereafter, the negative-acting-photosensitive material is exposed to ultraviolet light through substrate 100 and developed using conventional techniques. Because the longitudinal grooves 104 are the only means by which the negative-acting-photosensitive material is exposed, the negative-acting-photosensitive material over the stack is dissolved during a subsequent development process, leaving only longitudinal ridges 106 of negative-acting-photosensitive material disposed in grooves 104. Thus, it will be appreciated that by first patterning the sacrificial layer 102 and then exposing the negative-acting-photosensitive material through substrate 100 through longitudinal grooves 104 in the sacrificial layer 102, the sacrificial layer 102 acts as a photomask thereby allowing the negative-acting-photosensitive material to be lithographically patterned without the need for an additional masking step. In Figure 5 of the drawings, a structural layer 108 has been deposited on the stack and the sacrificial layer 102 has been removed, thus the layer 108 is supported by ridges 106. It will be appreciated that by using different photomasks it will be possible to fabricate support structures of any desired geometry. Thus instead of ridges, in other embodiments pillars or posts may be formed. The layer 108 is highly conductive and reflective and will typically contain aluminum and nickel.

[0014] Figure 6 of the drawings shows a subsequent stage in the manufacture of the MEMS device wherein the layer 108 is patterned into transversely extending strips. Figure 7 of the drawings shows the film stack with an oxide spacer layer 110 deposited on layer 108. Figure 8 of the drawings shows a stage in the manufacture of the MEMS device in which the oxide spacer layer 110 has been patterned. Figure 9 of the drawings shows a stage in the manufacture of the MEMS device in which a sealing film 112 is being applied with a pressure adhesive 114 over the entire structure to protect the structure from damage due to mechanical shock loading and to prevent particulates from interfering with the operation of the IMOD structures. The

sealing film 112 could be of a variety of materials such as thin metal films or polymeric films which have been coated with a metal or oxide film to provide hermeticity. Finally, Figure 10 shows the structure after it has been purged with XeF_2 gas to remove the remains of sacrificial layer 102. The edges of the structure are then sealed.

[0015] In other embodiments, instead of oxide layer 110 another layer of negative-acting-photosensitive material may be spun over oxide layer 110 and exposed through substrate 100 and using the techniques described above a further set of support structures may be formed. These support structures will provide support for other layers. It will be appreciated that the process may be repeated to build a MEMS structure having multiple layers or "floors" stacked one on top of the other wherein the floors are vertically spaced by support structures fabricated in accordance with the above techniques. One advantage of the present invention is that it provides a microfabrication technique which allows a mechanical support between two layers in an MEMS device to be precisely defined. This allows a clean, well-defined mechanical contact between the support and other structures within the MEMS device.

[0016] Further, the present invention uses a patterned layer on a substrate as a photomask to pattern another layer, thereby saving on a masking step.

[0017] Although the present invention has been described with reference to specific exemplary embodiments, it will be evident that the various modification and changes can be made to these embodiments without departing from the broader spirit of the invention as set forth in the claims. Accordingly, the specification and drawings are to be regarded in an illustrative sense rather than in a restrictive sense.

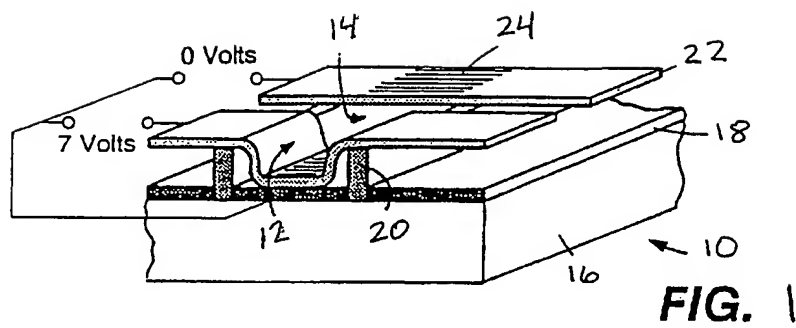
CLAIMS**What is claimed is:**

1. A microfabrication process for fabricating a microelectromechanical systems device, comprising:
 - depositing one or a stack of layers on a substrate;
 - patterning said one or a stack of layers;
 - depositing a middle layer on said one or a stack of layers; and
 - patterning the middle layer using said one or a stack of layers as a photomask.
2. The method of claim 1, wherein the substrate permits light to pass therethrough.
3. The method of claim 2, wherein the substrate comprises glass.
4. The method of claim 1, wherein patterning said one or a stack of layers comprises forming longitudinally spaced grooves therein.
5. The method of claim 4, wherein patterning said middle layer comprises exposing said middle layer to light passed through the grooves in the one or a stack of layers.
6. The method of claim 1, further comprising depositing top layer over said middle layer.
7. The method of claim 1, wherein said one or an uppermost layer of said stack of layers is a sacrificial layer.
8. The method of claim 1, wherein the said middle layer comprises a negative-acting-photosensitive material.

9. The method of claim 6, wherein said top layer comprises nickel and aluminum.
10. The method of claim 6, further comprising patterning said top layer.
11. The method of claim 5, further comprising developing said middle layer to form longitudinally spaced ridges in the said middle layer disposed in the grooves in said one or a stack of layers.
12. The method of claim 11, wherein said top layer is patterned to define transversely extending strips which are supported by the longitudinally spaced ridges in the said middle layer.
13. A method for fabricating a microelectromechanical systems device, the method of comprising:
 - a) depositing one or a stack of layers on a base layer, said one layer or an uppermost layer in said stack of layers being a sacrificial layer;
 - b) patterning said one or a stack of layers to provide at least one aperture therethrough through which said base layer is exposed;
 - c) depositing a photosensitive layer over said one or a stack of layers; and
 - d) passing light through said at least one aperture to expose said photosensitive layer.
14. The method of claim 13, wherein the base layer is a substrate layer.
15. The method of claim 13, wherein said light comprises ultraviolet light.
16. The method of claim 13, wherein said photosensitive layer comprises a negative-acting-photosensitive material.
17. The method of claim 13, further comprising depositing a structural layer over said photosensitive layer.

18. The method of claim 17, further comprising removing said sacrificial layer.
19. The method of claim 18, wherein said steps (a) to (d) are repeated at least once, wherein each structural layer defines the base layer.

1/10



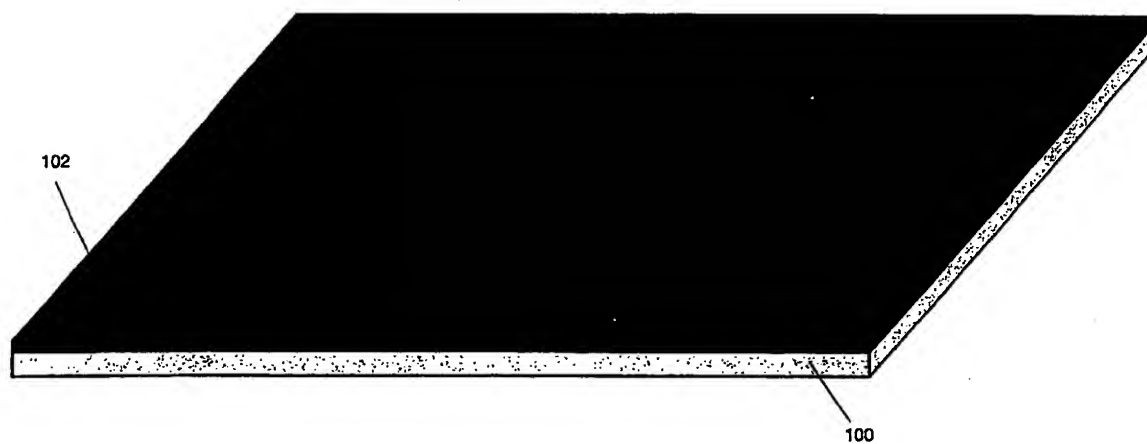


Figure 2

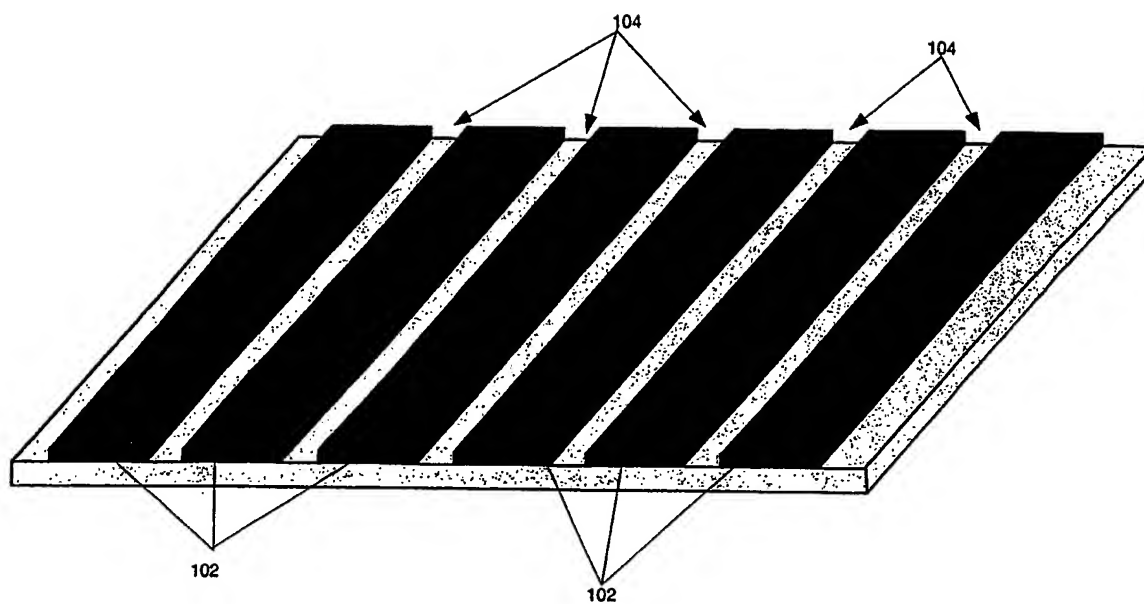


Figure 3

4/10

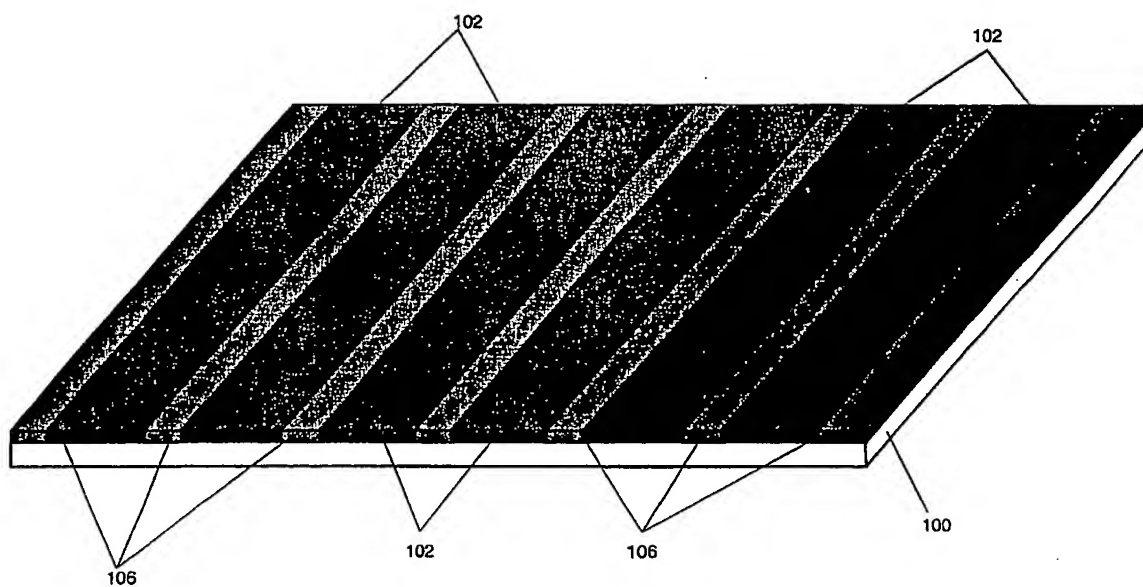


Figure 4

5/10

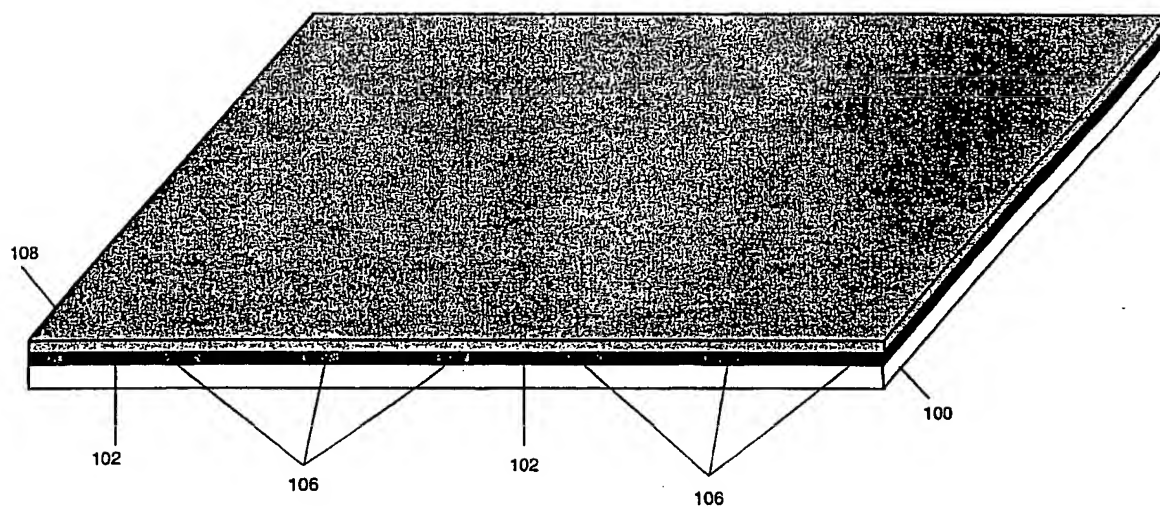


Figure 5

6/10

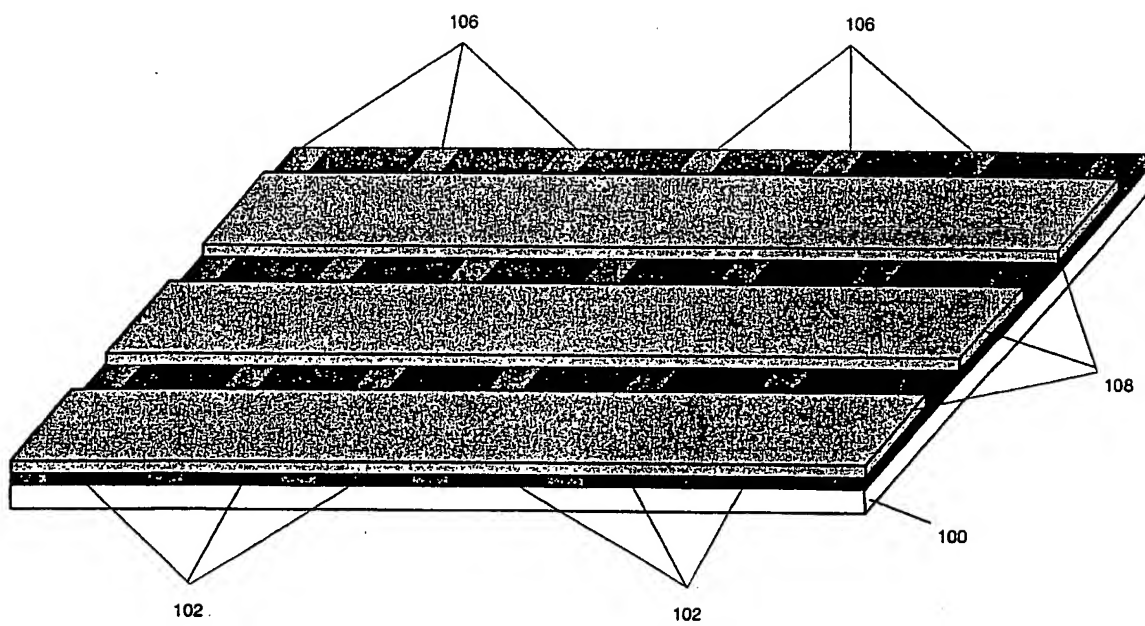


Figure 6

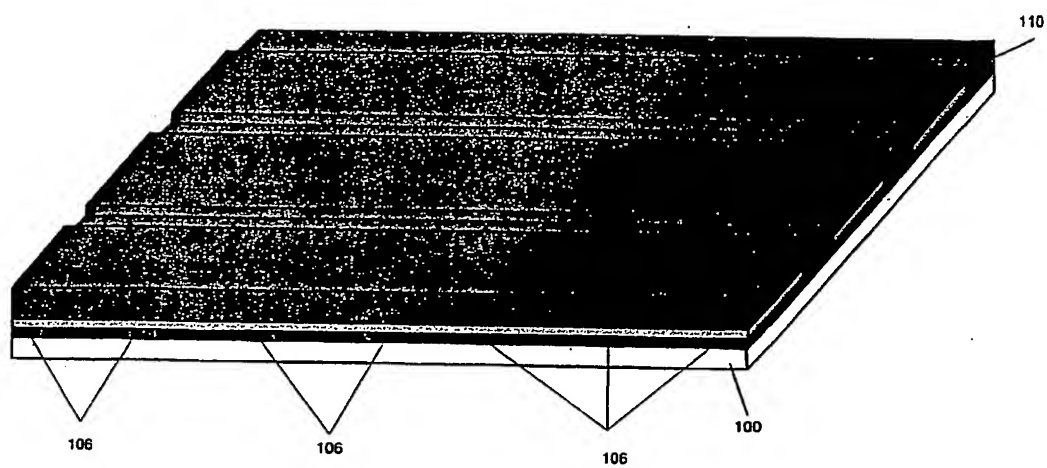


Figure 7

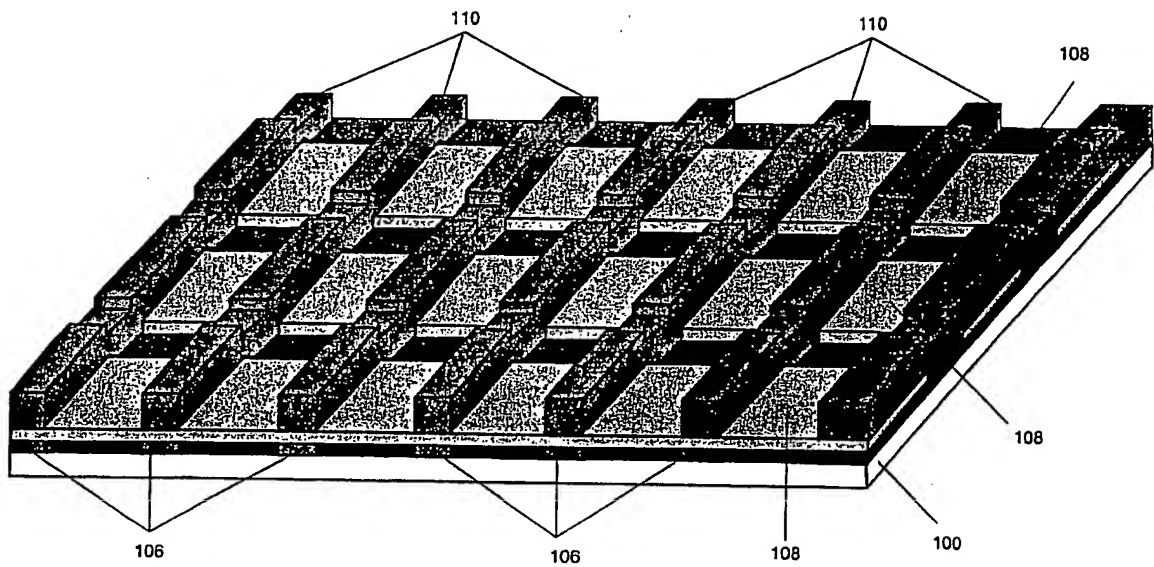


Figure 8

9/10

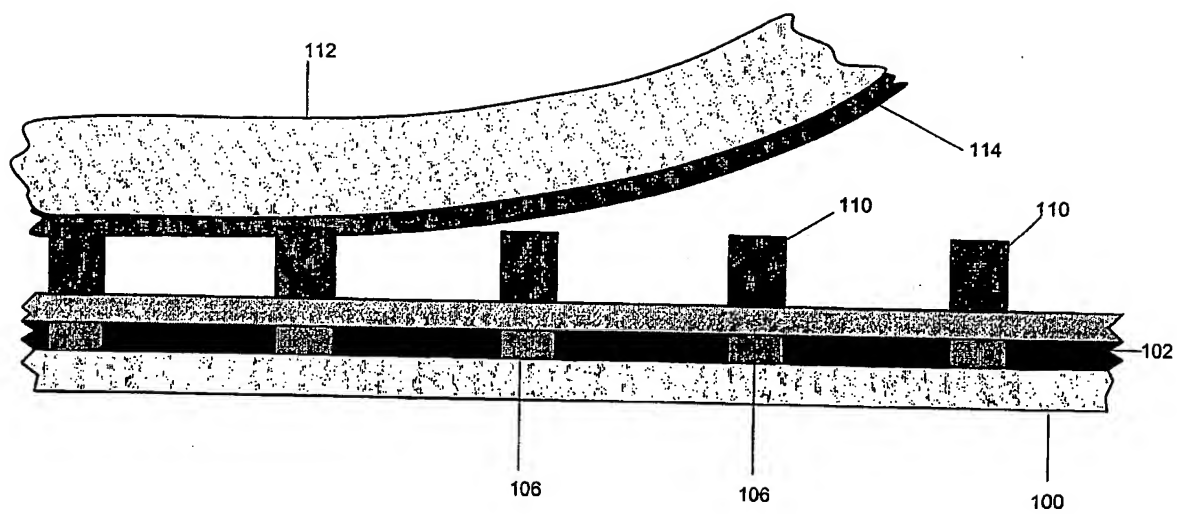


Figure 9

10/10

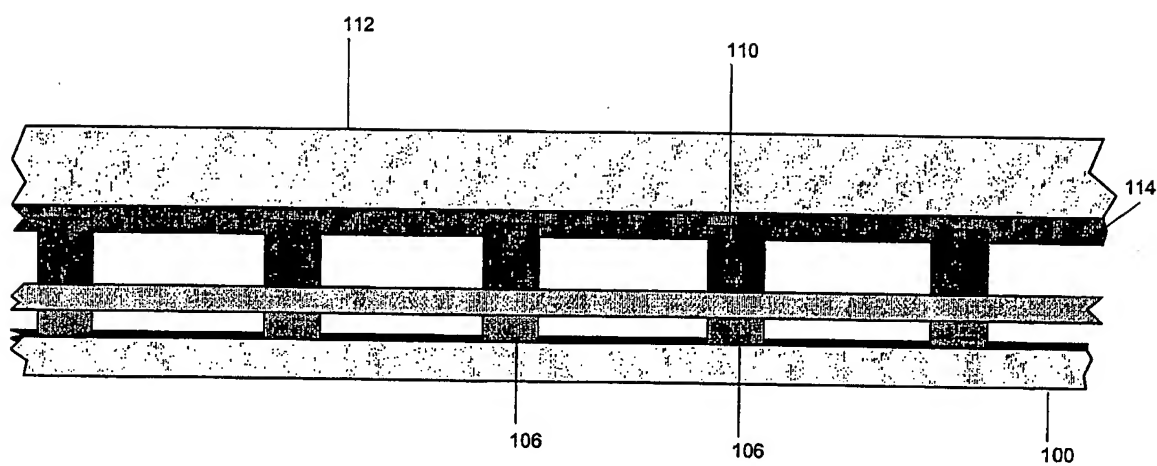


Figure 10

INTERNATIONAL SEARCH REPORT

International application No.

PCT/US02/13442

A. CLASSIFICATION OF SUBJECT MATTER

IPC(7) : G03F 7/20, 7/00
US CL : 430/311, 313; 216/41

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 430/311, 313; 216/41

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
WEST

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,674,757 A (KIM) 07 October 1997, col. 3, line 39 to col. 4, line 35 and claim 1.	1-19
Y	US 2001/0040649 A (OZAKI) 15 November 2001, paragraphs 0010 and 0011, figures 15A, 15B, 17A and 17B.	1-19

☐ Further documents are listed in the continuation of Box C.

☐ See patent family annex.

* Special categories of cited documents:	
"A" document defining the general state of the art which is not considered to be of particular relevance	"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"E" earlier application or patent published on or after the international filing date	"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"O" document referring to an oral disclosure, use, exhibition or other means	"&" document member of the same patent family
"P" document published prior to the international filing date but later than the priority date claimed	

Date of the actual completion of the international search

23 August 2002 (23.08.2002)

Date of mailing of the international search report

13 SEP 2002

Name and mailing address of the ISA/US
Commissioner of Patents and Trademarks
Box PCT
Washington, D.C. 20231

Facsimile No. (703)305-3230

Authorized officer

Kathleen Duda

Telephone No. 703-308-0661

**This Page is Inserted by IFW Indexing and Scanning
Operations and is not part of the Official Record**

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☐ **BLACK BORDERS**
- ☐ **IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- ☐ **FADED TEXT OR DRAWING**
- ☐ **BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- ☐ **SKewed/SLANTED IMAGES**
- ☒ **COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- ☐ **GRAY SCALE DOCUMENTS**
- ☐ **LINES OR MARKS ON ORIGINAL DOCUMENT**
- ☐ **REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- ☐ **OTHER:** _____

IMAGES ARE BEST AVAILABLE COPY.

As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.